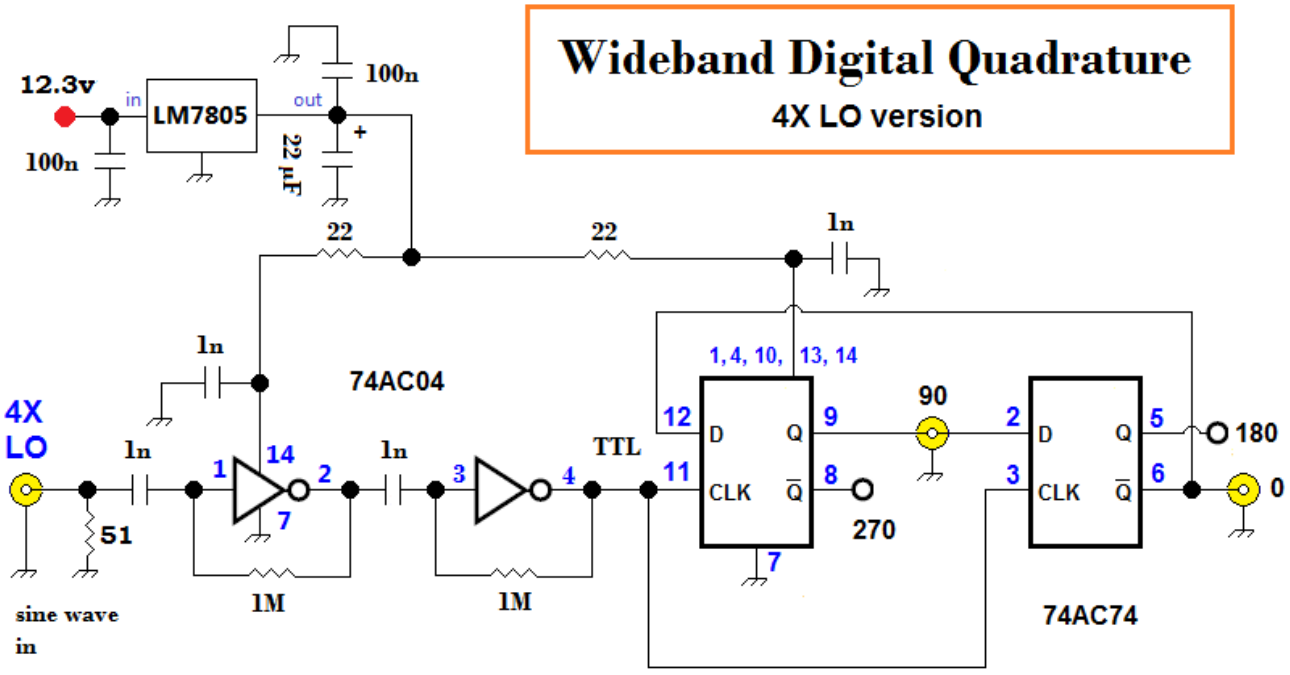
In search of a wideband digital quadrature for a ZIF receiver

Feb 6, 2016 --- VE7BPO Discussion document

In many homebrew, discrete, digital quadrature's, a pair of D flip flops are clocked together to form a walking shift register. The input LO gets divided by 4 and the output looks symmetrical [50 – 50 duty cycle]. The input to each clock takes an identical route through the D-FF and this results in a low I-Q channel phase error.

Here's 1 I built below. My signal source in all cases = a low distortion sine wave with and output power of 10 dBm and Z of 50 ohms. As shown below, 2 inverters with negative feedback square up the sinewave with the hope of getting a 50% duty cycle into the flip-flops.

Duty cycle = the ratio of the pulse width to the period time --- or simply, in this application, we want the digital stage on for half of the time and off during the other half.

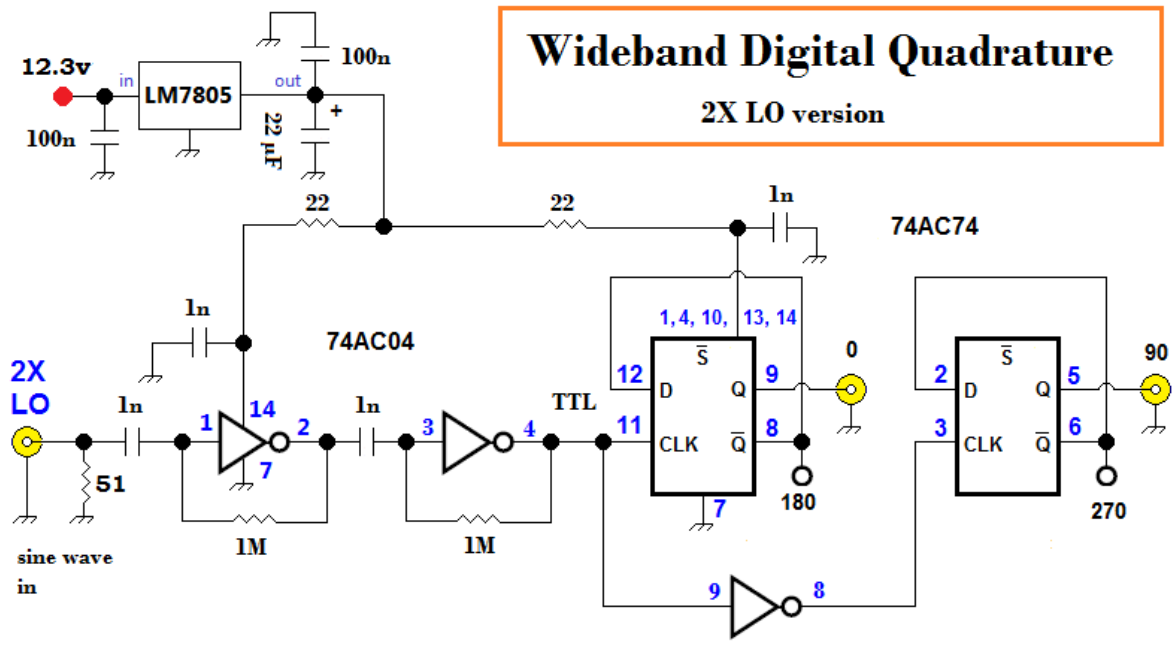


If signal generator has square wave output with 50/50 duty cycle and TTL -- just connect to flip-flop

Above --- A digital quadrature that requires a divide by 4 LO

I sought to make a digital quadrature that only divides the LO by 2. Without the divide by 4, I discovered the input signal duty cycle seems critical. The problem with using digital ICs for creating quadrature waveforms is the phase uncertainty at higher frequencies. Variations in switching time with temperature and device choice can easily be in the low nanosecond range -- which lies in the range of ~ 20 to 50 degrees at 50 MHz! Then you have to consider the propagation delay imposed by the inverter used to feed the second flip flop's clock input.

Here's my first version of the LO/2 or quadrature. Also called a switch tail ring counter.



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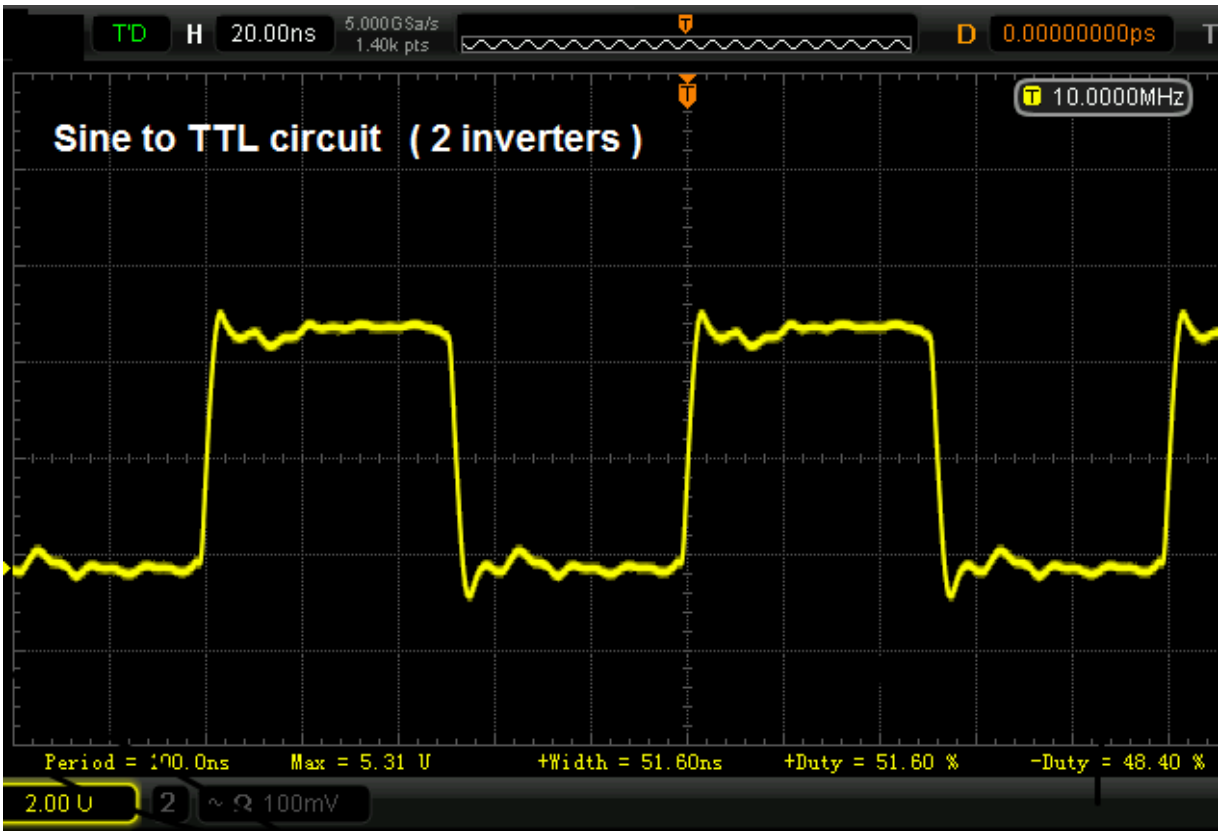

Above – The output of the 2 inverters when driven with a sine wave with the D-FF disconnected. Not quite a 50/50 duty cycle.

Scroll for more……

Above -- the quadrature output with the sine wave oscillator set to 10 MHz. I measured a 3.13 degree phase error. That would trash opposite sideband suppression on 30 meters. I then investigated varying the duty cycle on the sine wave to square wave converter. Although digital circuits with feedback that allow a varied duty cycle may be found in the literature; to alter the duty cycle, I went to a simple differential circuit I learned about from Charles Wenzel.

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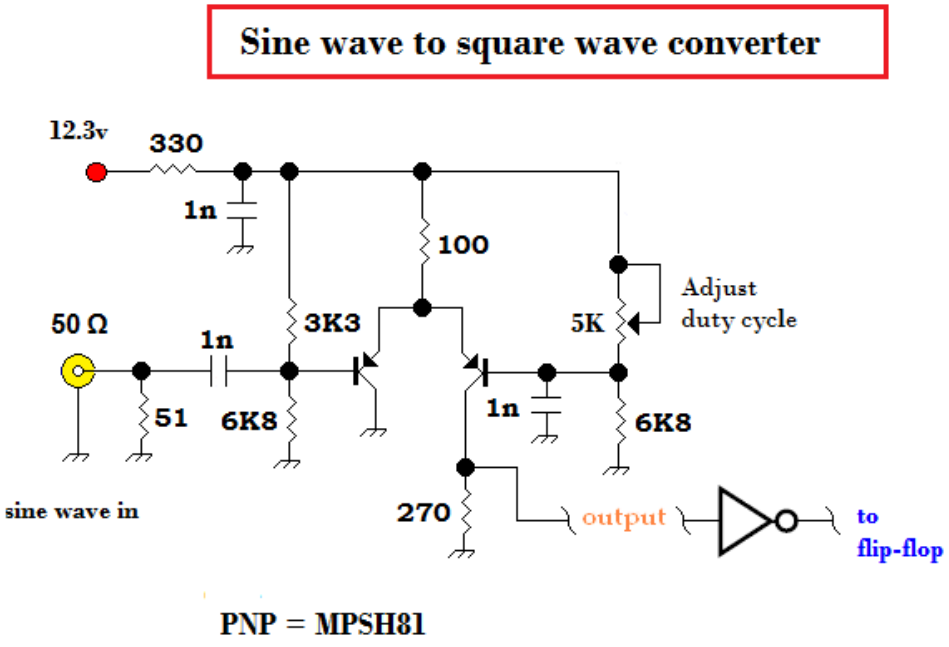
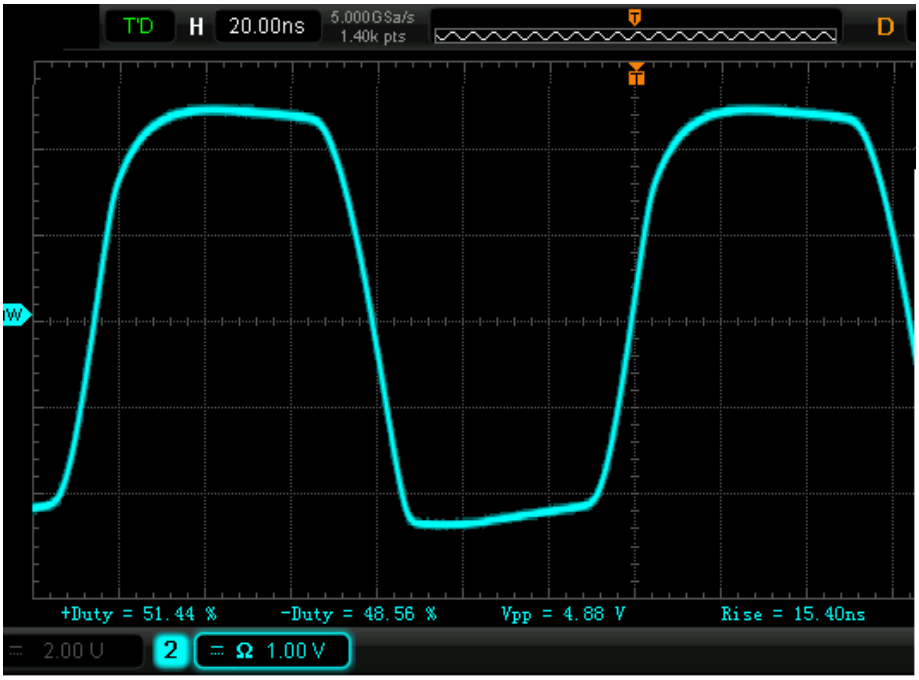
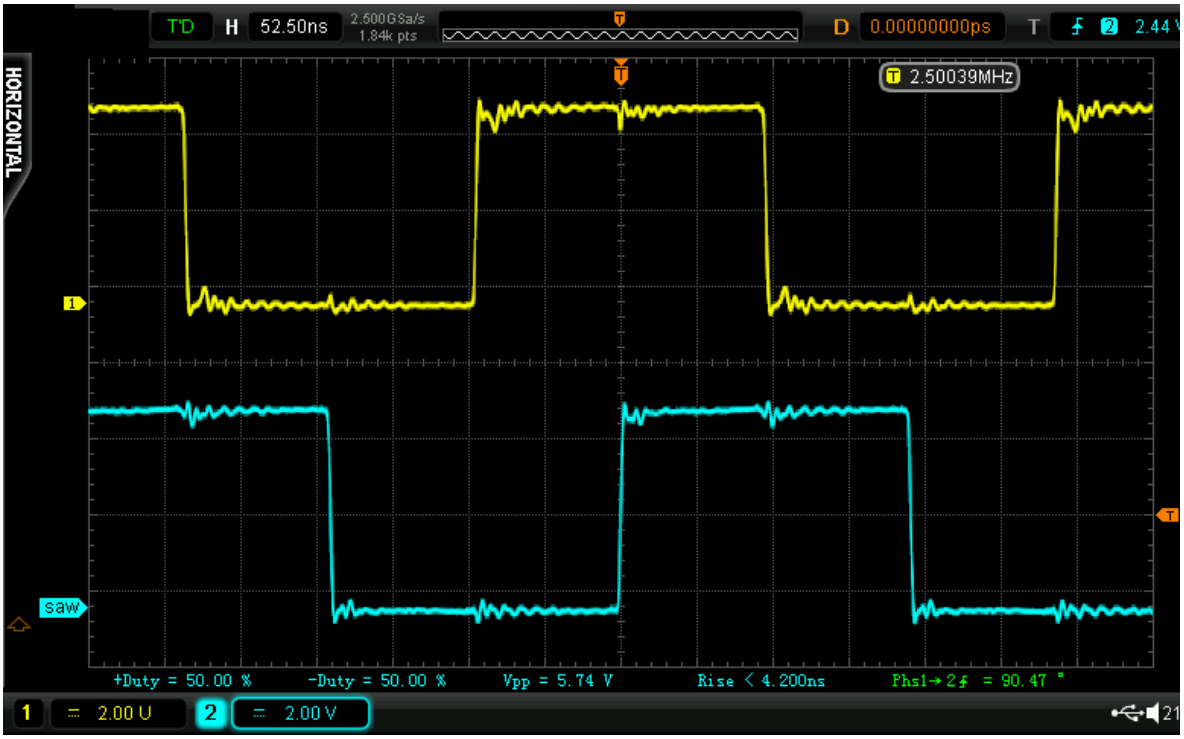


Above – Differential circuit. By placing a trimmer pot on the BJT with its base AC grounded, I found you can vary the duty cycle a little.



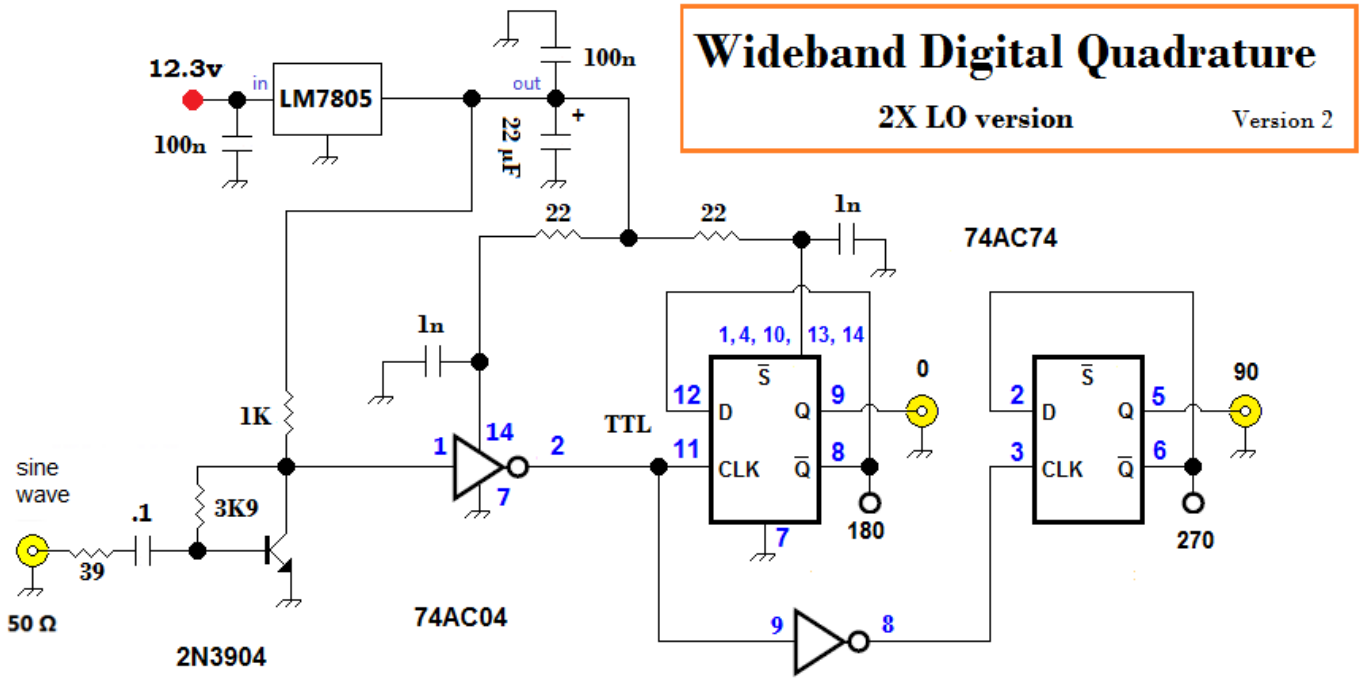
Above - A 51.44 – 48.56 duty cycle from the differential circuit with 1 setting of the 5K trim pot

Above – The duty cycle corrected towards 50%. Then, I connected up **1** inverter from a 74AC04 used in the quadrature stage to square it up.

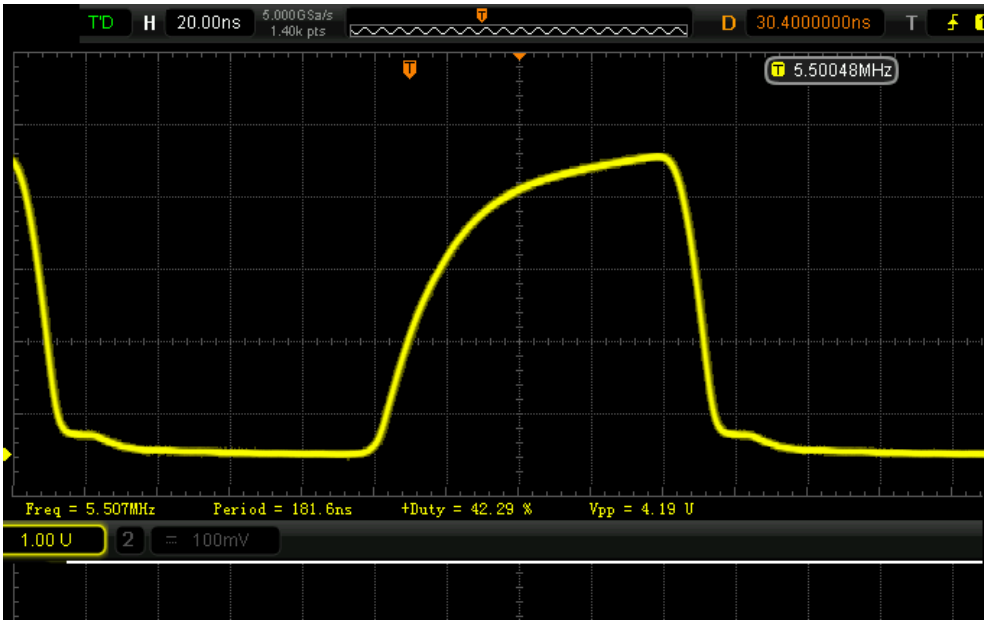


Above --- The quadrature output where LO = 5 MHz. I got a little closer to my goal of 0 degrees phase error. I was able to slightly tweak for lower phase error with the pot on the differential

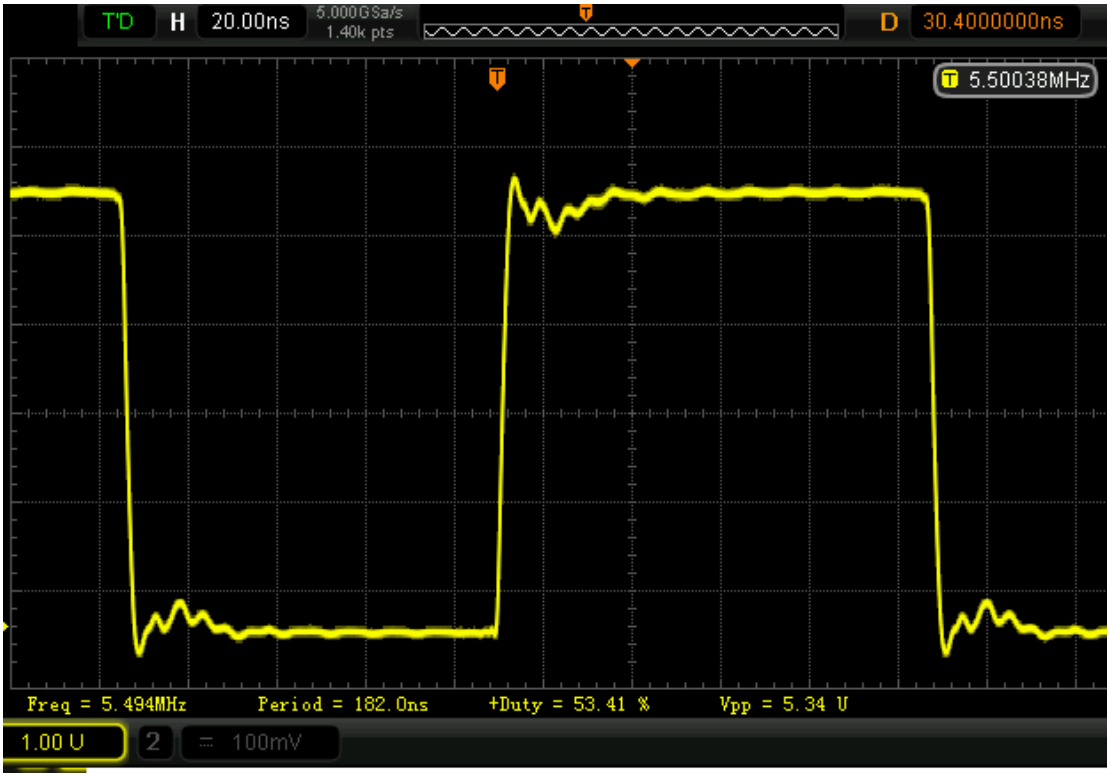
pair shown earlier. I could not get to 0 degrees error however. Even the wiring length from the inverter output to the clock inputs seemed to change the phase error. It shouldn't. For phase shift versus wire length: at 10 MHz, using a conduction velocity of ~2/3 light then 1 degree is about 56 mm of wire.



Above --- Version 2 of the 2X LO with a BJT sine to square wave converter and a single inverter to square it up.



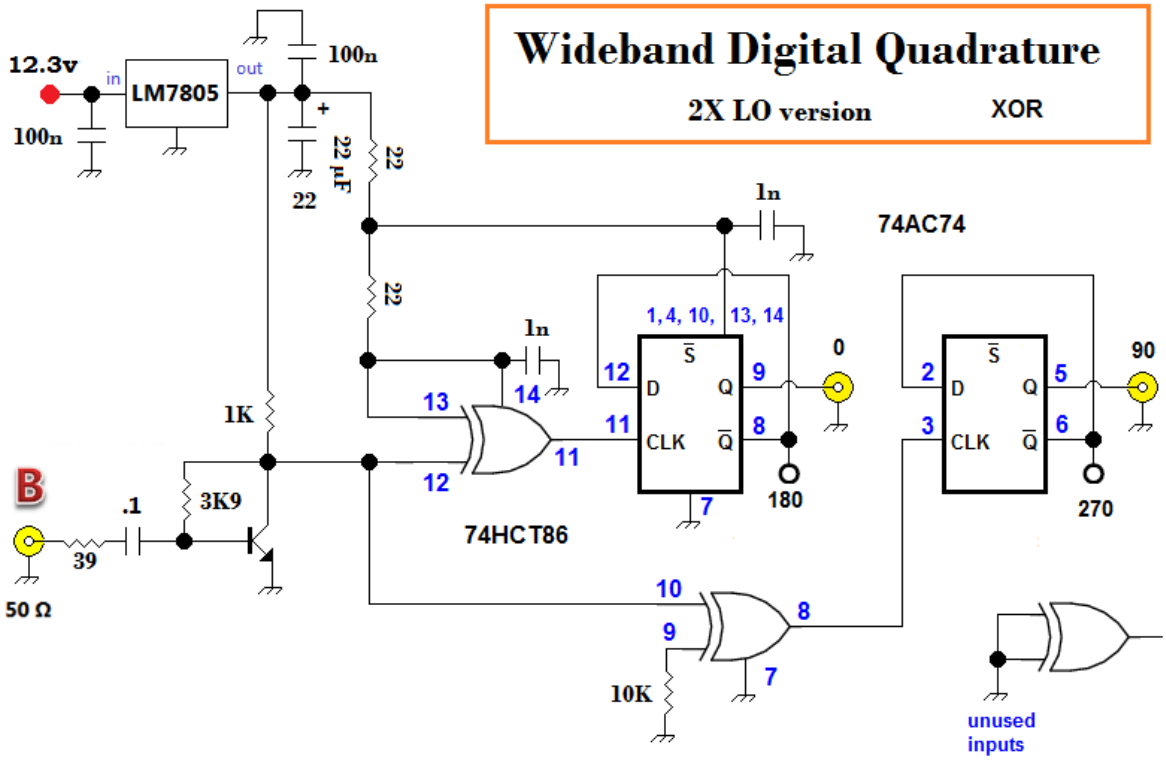
Above – The output from the BJT sine to square wave converter.



The output from the inverter that follows the BJT. By tweaking the sinewave signal source drive pot (between 8 - 10 dBm), I was able to affect the duty cycle of the square wave output

Above – At frequencies ~2- 5 MHz, I was able to obtain zero degrees phase error by tweaking the sine wave signal source. Moving above 5 MHz, phase error slowly crept in.

Some suggested a XOR input buffer. I built it below:



Above --- The only working XOR chip I had = the 74HC86. This puts a XOR gate on each of D-FF clock input. Sadly, this did not solve the problem. While I measured 0 phase error at ~ 2 or so MHz, this stage suffered the same issues as the others -- and if anything, phase error worsened with frequency changes [might have been the 74HC series versus 74AC series?]. Drive level and frequency changes up to 10 MHz maximum altered the phase error as much as 9 degrees. I even tried an extra buffer made with a XOR stage after the BJT sine to square converter – it didn't help.

The 2X LO circuit seems disappointing. It took a huge amount of bench work to make something that works marginally. I'm not even that interested in HF --- and I'm uncertain if my results are even reproducible. Not a total waste however – I learned a ton. Phase domain experiments present quite a challenge.